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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,891	01/21/2004	John Atkinson Fifield	BUR920030077US1	1890

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,891	FIFIELD ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9 and 13-15* is/are rejected.

7)☒ Claim(s) *7 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 5/3/05. Claims 1 and 7 – 9 have been amended. Claims 1 – 15 are pending on this office application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> ((b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States

3. Claims 1 – 6, 8, 9, and 13 - 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Botti et al. U.S. Patent No. 5,621,357.

Regarding claim 1, Fig. 1 and 4 of Botti et al. discloses a differential amplifier circuit comprising: a first differential amplifier (Q1, Q2) for receiving a pair of differential input signals (-,+) to generate a first output (Irn); a second differential amplifier (Q5, Q6) for receiving said pair of differential input signals (-, +) and generate a second output (Irp) and a summing circuit (Qpf, Qnf) for summing (Out) said first output (Irn) of said first differential amplifier (Q1, Q2) and said second output (Irp) of said second differential amplifier (Q5, Q6) to provide a common output (Iout) for said differential amplifier circuit, and a reference voltage generating circuit (Qpref, Qnref) for providing a reference voltage signal (Vref) to said summing circuit (Qpf, Qnf), wherein said reference voltage circuit is a differential amplifier (Qpref, Qnref).

Regarding claim 2, wherein said first differential amplifier is an n-channel differential amplifier (Q1, Q2).

Regarding claim 3, wherein said first differential amplifier (Q1, Q2) includes a pair of n-channel transistors (Q1, Q2) for receiving said pair of differential input signals (-, +) respectively.

Regarding claim 4, wherein said second differential amplifier (Q5, Q6) is a p-channel differential amplifier.

Regarding claim 5, wherein said second differential amplifier (Q5, Q6) includes a pair of p- channel transistors (Q5, Q6) for receiving said pair of differential input signals (-, +) respectively.

Regarding claim 6, wherein said summing circuit (Qpf, Qnf) is an n-channel (Qnf) differential amplifier.

Regarding claim 8, wherein said reference voltage (Qpref, Qnref) is a p-channel differential amplifier (Qpref).

Regarding claim 9, wherein said reference voltage circuit (Qpref, Qnref) receives an active low enable signal (Since reference voltage generation circuit Qpref is a p-channel amplifier, therefore the control gate of Qpref must receive a low signal to active or enable the Qpref).

Regarding claim 13, wherein said first differential amplifier (Q1, Q2) receives a gate control voltage (Voltage at the gate of Q3, Q4) to control the current through an n channel transistor (current flowing through Q1) within said first differential amplifier (Q1,

Q2) in a consistent and predictable manner using a current mirror technique (Q3 and Q4 are current mirror).

Regarding claim 14, said second differential amplifier (Q5, Q6) receives a gate control voltage (voltage at the control gate of Q7, Q8) to control the current through a p-channel transistor (Q5) within said second differential amplifier (Q5, Q6) in a consistent and predictable manner using a current mirror technique (Q7 and Q8 are current mirror).

Regarding claim 15, wherein said summing circuit (Qpf, Qrf) receives a gate control voltage (Voltage at the gate of Qnref) to control the current through an n-channel transistor (Qnf) within said summing circuit (Qpf, Qnf) in a consistent and predictable manner using a current mirror technique (Qnref, and Qnf is a current mirror).

Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Allowable Subject Matter

5. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior does not teach or suggest wherein the summing circuit includes an n-channel transistor pair, wherein a first transistor of the n-channel transistor pair receives the voltage reference signal from the reference voltage

generation circuit, wherein a second transistor of the n-channel transistor pair receives combined output signal from the first output the of the first differential amplifier and the second output of the second differential amplifier.

6. Claims 10 - 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claim 10, the prior art does not teach, wherein the first and second differential amplifiers received an active low ENBALE-N signal.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

6/12/05

Linh Van Nguyen

Art Unit 2819

PEGUY JEANPIERRE
PRIMARY EXAMINER